OVP center control protocol

Support model:

OVP-H8XL,OVP-H4XL,OVP-H2XL,OVP-M4X,OVP-M2X,OVP-L2X,OVP-M1X,OVP-L1X,OVP-M4D, OVP-M2D,OVP-M2DA.

1. Protocol format

In order to meet the reliability and non-real-time nature of serial communication, the protocol is divided into two layers. They are the PHY0 layer and the PHY1 layer. The PHY0 layer contains all the data of the PHY1 layer.

1.1 PHY0 layer

The main function of PHY0 is to indicate the start and end of a data frame. Use 0xA5 to indicate the beginning of a data frame, and 0x5A to indicate the end of a data frame. Between the frame start tag (0xA5) and the frame end tag (0x5A) is the PHY1 layer data. All 0xA5 and 0x5A in the PHY1 layer data must be escaped to ensure that the frame start tag (0xA5) and the frame end These two characters will not appear between the mark (0x5A). In addition, when 0xA5 is used as the start of a data frame, there can be multiple. Its structure is shown in the figure below.

1.1.1 PHY0 data escape

The PHY1 layer to the PHY0 layer must be escaped, the purpose is to remove the character data 0x5A and 0xA5 in the PHY1 layer. The PHY0 layer to PHY1 should also be escaped, the purpose is to restore the character data 0x5A and 0xA5 in the PHY1 layer.

The encapsulation process from PHY1 to PHY0:

a) If 0xA5 is encountered in PHY1, it will be escaped as 0xA6, 0x02, if 0xA6 is encountered, it will be escaped as 0xA6, 0x01

b) If 0x5A is encountered in PHY1, it will be escaped as 0x5B, 0x02, if 0x5B is encountered, it will be escaped as 0x5B, 0x01

PHY0 to PHY1 unpacking process:

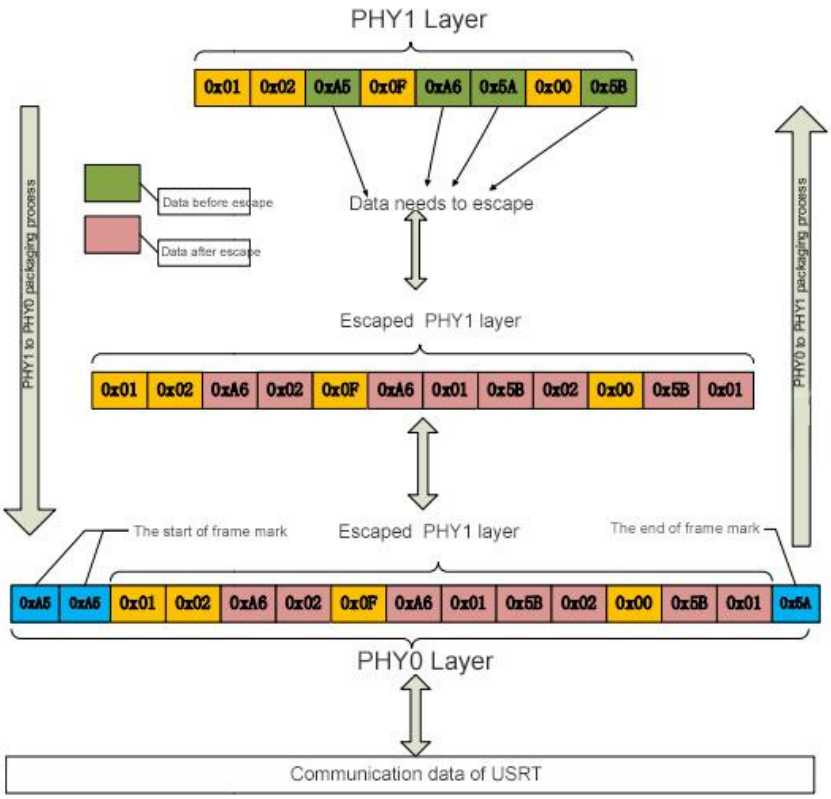
a) If two consecutive bytes are 0xA6, 0x02, the inverse meaning is 0xA5

b) If you encounter two consecutive bytes as 0xA6, 0x01, the inverse meaning is 0xA6

c) If two consecutive bytes are 0x5B, 0x02, the reverse meaning is 0x5A

d) If you encounter two consecutive bytes as 0x5B, 0x01, the reverse meaning is 0x5B

1.1.2 Encapsulation and unpacking of data



1.2 PHY1 layer

The data of the PHY1 layer is the data actually parsed by the controller. It includes two parts: the header and the data area. Among them, the header contains the control address, version number, command value, etc. The data part contains specific configuration data information.

PHY layer structure

head	Data field	CRC

1.2.1 Head of PHY1 layer

Head of PHY1 layer instruction:

parameters	Length	Default value	Description
Dst_addr	2	0	Target address
Src_addr	2	0	Source address

Version	1	0x10	Protocol version number The default is 0x10
sequence number	1	0x00	Frame sequence number. The returned result must be consistent with it. In order to avoid frame conflicts when the MCU communicates with the video processor. When the MCU is the master and the video processor is the slave, the value range is 0xE0 to 0xEF. When the video processor is the master and the MCU is the slave, the value range is 0xD0 to 0xDF. For these two values, PC software cannot be used.
Controller Class	1	0x00	Controller category, which represents a type of controller. 0x08-video processor

			0xFF——Wild card, all devices respond to the current command
Reserved0	1	0x00	Reserved value, the default is 0.
Reserved1	1	0x00	Reserved value, the default is 0.
command	1	0xB0	Command word
Data field	N		Data field
CRC	1		Check value Starting from Dst_addr, to the exclusive OR check value of the data field.

Mark:communication address

Adress	instruction
0xF010	pc address
0xF100	Video processor

2. Communication instruction

2.1 Serial communication

Default baud：115200kps

2.2 Ethernet communication

1) Direct link mode：

Default IP adress：192.168.192.10；default port：5005

Mark ：The video processor and the host must be in the same network segment：192.168.192.xxx

2) Fix IP mode：

Modify the IP address and port number of the video processor through PC software.

Mark : When setting a fixed IP, only one video processor can be connected to the LAN.

3. Register setting command **0x31.**

format: head 31 sign addr1 data1_L data1_H … addrN dataN_L dataN_H CRC 5A

Instruction ：

Multiple values (one byte/address + two bytes/value) are written into the specified address in the DSP ram table.

PC->MCU->DSP: head 31 sign addr1 data1_L data1_H ... addrN dataN_L dataN_H CRC 5A.

DSP->MCU: According to different processing methods, DSP sets the status (status bit) and responds, the format is as follows: If the command is correct and the value of the DSP register is the same as the value set by the MCU, set status to 0 and reply:
head status 31 CRC 5A, if the command is wrong, the status bit will be set to 1, and the original value will be updated to the MCU.
head status 31 addr1 data1_L data1_H ... addrN dataN_L dataN_H CRC 5A

If the command causes other registers to be updated, the DSP will send the updated registers to the MCU. head status 31 addr1 data1_L data1_H ... addrN dataN_L dataN_H CRC 5A

A single value (one byte/address + two bytes/value) is written into the specified address in the DSP ram table.
Some single-value commands do not reply (please refer to RAM table). Other commands that need

to be replied are executed according to the reply of write multi-value commands.
MCU->PC: MCU reply command number: head status 31 CRC 5A (Note: in all commands replying to the PC, the response byte (Status) is inserted after the frame header, which is consistent with the synchronization protocol framework).

sign: Execution sign byte
Bit7: Execution Bit: 1: Execution; 0: Not Execution Bit6: Frame End Bit: 1: End; 0: Not End
Bit0~Bit5: Frame Number: Start from 0

4. Register read command **0x36.**

Description: PC reads multiple values in DSP ram table through MCU

Format: Frame-Head 36 addr LenL lenH CRC 5A (addr represents the starting address of reading, Len represents the number of data read)

MCU->PC: len data starting from the address addr are sent to the PC in the format of (address + data low + data high).
DSP return: Frame-Head state 36 addr1 data1_L data1_H … addrN dataN_L dataN_H CRC 5A

5. Signal source switch

5.1 Format：

Frame-Head 31 sign Addr Data_L Data_H CRC 5A

Instruction：

Frame-Head（head of frame)：A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0

31：Single value write subcommand sequence number

Sign: Execution sign, the single value register is 0xC0. Addr: 15-screen 1signal source, 1D-screen 2 signal source Data_L: The corresponding values are as follows.

0x00: DP1

0x01: DP2

0x02: HDMI1

0x03: HDMI2

0x04: DVI1/DVI

0x05: DVI2/EXT
0x06: VGA
0x07: CVBS
0x08: Reserved value, the default is 0.
0x09: USB

Data_H：00
CRC：XOR check
value5A：end
the frame?

Video processor -> PC
Accept the error：Not deal
Accept the correct ：Reply to relevant source data

5.2 Example：
Switch the window 1
source to DP1PC -> Video
processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15(Addr:window 1 signal source) 00(Data_L:DP1 signal source item number)
00 CRC(Total XOR check) 5A
注：CRC 为“00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 00 00”XOR check value

1) Switch window 1 source
a) DP1 signal source
PC -> Video processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 00 00 5D 5A
b) DP2 signal source
PC -> Video processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 01 00 5C 5A
c) HDMI1 signal source
PC -> Video processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 02 00 5F 5A
d) HDMI2 signal source
PC -> Video processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 03 00 5E 5A
e) DVI1 signal source
PC -> Video processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 04 00 59 5A
f) EXT signal source
PC -> Video processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 05 00 58 5A
g) VGA signal source
PC -> Video processor
A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 06 00 5B 01 5A
h) CVBS signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 07 00 5B 02 5A

i) USB signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 15 09 00 54 5A

2) switch the window 1 source to DP1 2 signal source

a) DP1 signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 00 00 55 5A

Video processor -> PC

A5 A5 A5 10 F0 00 F1 10 00 08 00 00 B0 00 31 88 5A

b) DP2 signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 01 00 54 5A

c) HDMI1 signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 02 00 57 5A

d) HDMI2 signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 03 00 56 5A

e) DVI1 signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 04 00 51 5A

f) EXT signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 05 00 50 5A

g) VGA signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 06 00 53 5A

h) CVBS signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 07 00 52 5A

i) USB signal source

PC -> Video processor

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 1D 09 00 5C 5A

Mark:

1) When switch the window 1 source to DP1 2 signal source, firstly should open the corresponding window to take effect.
2) OVP-M4X,OVP-M2X,OVP-L2X,OVP-M1X,OVP-L1X,OVP-M4D,OVP-M2D,OVP-M2DA Video processor not support the window 2 or switch signal source.
3) Different model of Video processor support different signal source (check user manual), If the signal source switching command that is not supported by the current model is sent, it cannot take effect and the response command is abnormal (see below).
4) Video processor -> PC

a) switch the window 1 source to DP1 signal source command correct reply:
A5 A5 A5 10 F0 00 F1 10 00 08 00 00 B0 00 31 88 5A

b) switch the window 1 source to DP1 signal source command abnormal reply:
A5 A5 A5 10 F0 00 F1 10 00 08 00 00 B0 05(ACK Error type: Invalid command) 31 8D 5A

c) No reply: The command format is abnormal.

5) The interval of repeated frame transmission is 3 seconds.

6. User mode switch

6.1 Format

Frame-Head 31 sign Addr Data_L Data_H CRC 5A

Instruction:

Frame-Head (Frame head): A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0

Sign: Execution mark, the single value register is 0xC0.

Addr: 0x36/0x35

Data_L:

The low byte of 0x36: 0~7 is the user-defined mode of 1~8; 16~23 is the user-defined mode of 9~16; 8 is the current mode, including the real-time parameters in the current state, when the user modifies any parameter After that, User mode will be set to the current mode.

Low byte of 0x35: Video processor that only supports multi-screen can be expanded to 16 User modes (some models are not yet open)

BIT0 ~ BIT7: Custom mode save/clear bit,range:
0x00~0xFF BIT0:User mode9 (1->saved, 0-> not saved)
BIT1:User mode10 (1->saved, 0->not saved) BIT2:User mode 11 (1->saved, 0->not saved) BIT3:User mode 12 (1->saved, 0->not saved) BIT4:User mode 13 (1->saved, 0->not saved) BIT5:User mode 14 (1->saved, 0->not saved)
BIT6:User mode 15 (1->saved, 0->not saved) BIT7:User mode 16(1->saved, 0->not saved)

Data_H:

0x36 High byte:

BIT8 ~ BIT15 : Custom mode save/clear bit,Rang :
0x00~0xFF BIT8:User mode0 (1->saved , 0-> not saved)
BIT9:User mode1 (1->saved , 0->not saved) BIT10:User mode 2 (1->saved, 0->not saved) BIT11:User mode 3 (1->saved, 0->not saved) BIT12:User mode 4 (1->saved, 0->not saved) BIT13:User mode 5 (1->saved , 0->not saved)
BIT14:User mode 6 (1->saved , 0->not

saved） BIT15:User mode 7 (1->saved， 0->not saved）

User mode parameter setting: For each different User mode (MODE) setting, the parameters that need to be saved are saved in the DSP, the MCU sends the specified User mode to the DSP, and the DSP loads the specified mode data and completes the initialization. .

User mode includes parameters: brightness, contrast, saturation, dynamic brightness, signal source interception parameters (start/width/height), hot backup settings, multi-screen input signal source settings (screen ID/rotation/signal source) , Custom screen 1 XY start/height width, switch/signal source/rotation, custom screen 2 XY start/height width, switch/signal source/rotation, custom screen 3 XY start/height width , Switch/signal source/rotation, custom screen 4 XY start/height and width,

Switch/signal source/rotation
User mode cancellation: After setting the application mode and LED screen parameters, all User modes in the DSP will be cleared

Mode storage mode: in the high byte, set the bit position of the specified mode to 1, and the remaining bits are 0, (the low byte of 0x36 is set to
0xFF), for example, to save the current data to mode 0, the data sent using the single value setting command is 0x01FF

Mode clearing method: In the high byte, the bit position of the specified mode is set to 0, and the remaining bits are set to 1, (the low byte of 0x36 is set to
0xFF), for example, to clear the data in mode 0, the data sent using the single value setting command is 0xFEFF

Mode selection method: the high byte is set to 0, and the low byte is set to the mode number. For example, if fixed mode 1 is selected, the data sent using the single value setting command is 0x0009

CRC：XOR check value

6.2 Example：

Calling to saved **(**User mode **1~8：0~7)**

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 mode number(0~7,16~23) 00 CRC(Total XOR Check) 5A

PC -> Video processorUser mode1

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 00 00 7E 5A

User mode 2

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 01 00 7F 5A

User mode 3

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 02 00 7C 5A

User mode 4

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 03 00 7D 5A

User mode 5

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 04 00 7A 5A

User mode 6

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 05 00 7B 5A

User mode 7

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 06 00 78 5A

User mode 8

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 07 00 79 5A

User mode 9

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 10 00 6E 5A

User mode 10

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 11 00 6F 5A

User mode 11

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 12 00 6C 5A

User mode 12

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 13 00 6D 5A

User mode 13

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 14 00 6A 5A

User mode 14

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 15 00 6B 5A

User mode 15

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 16 00 68 5A

User mode 16

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 17 00 69 5A

Note:

1) Before calling User mode, you need to save the required configuration to User mode through PC software.
2) Modifying the LED screen parameters or factory reset will clear all User modes.
3) The interval of repeated frame transmission is 3 seconds.

5.3 Reference code **-Calling to the saved user mode 1**

```
void SendUserModeChangeData(void)
{
        BYTE addr_no = 0x12;
        BYTE vp_datalow = 00;
        BYTE vp_datahigh = 01;
        BYTE vp_cmd = 0x31;
        BYTE Head_DataBuff[12];
        BYTE Start_DataBuff[1];
        BYTE Real_DataBuff[1];
        BYTE crc,i;



        Head_DataBuff[0] = 0x00; //The lower 8
        bits of the target address
        Head_DataBuff[1] = 0xF1; //The upper 8
        bits of the target address
        Head_DataBuff[2] = 0x10; //The lower 8
        bits of the source address
        Head_DataBuff[3] = 0xF0; / /High 8
        bits of the source address
        Head_DataBuff[4] = 0x10; //Protocol
        version number
        Head_DataBuff[5] = 0xD0; //Frame
        serial number

        Head_DataBuff[6] = 0x08;        //controller
```

```
categoryHead_DataBuff[7] = 0x00;
                                //Reserved
value, the default is 0.value
Head_DataBuff[8] = 0x00;        //Reserved
value, the default is 0.value
Head_DataBuff[9] = 0xB0;        //video
processor command
Head_DataBuff[10] = vp_cmd; //pkg_cmd;
Head_DataBuff[11] = 0xC0;  //sign;
```

```
Start_DataBuff[0]          =          0xA5;
                                    //pkg_h
ead;     Start_DataBuff[0]     =     0xA5;
                                    //pkg_h
ead;     Start_DataBuff[0]     =     0xA5;
                                    //pkg_h
ead;

SendDataByte( Start_DataBuff[

0] ); for ( i = 0; i < 12; i++)
        {
            SendDataByte( Head_DataBuff[i]);

          }


crc = Head_DataBuff[0];
          for ( i = 1; i < 12; i++)
           {
                crc ^= Head_DataBuff[i];
           }


SendDataByte(addr_no);
SendDataByte(vp_datalow);
SendDataByte(vp_datahigh);

crc ^=   addr_no;
crc ^=
vp_datalow;
crc ^= vp_datahigh;

SendDataByte(crc);

Real_DataBuff[0] = 0x5A; //send end-code

SendDataByte( Real_DataBuff[0] );



}
```

Note: SendDataByte() is a function for sending a single byte at the bottom layer.

7. Brightness command

7.1 Format

Frame-Head 31 sign Addr Data_L Data_H CRC 5A

Instruction：

Frame-Head（frame head)：A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0

Sign: Execution sign, single value register is

0xC0. Addr: 0x06

Data_L: the low byte of the brightness value

Data_H: the high byte of the brightness value

CRC: XOR check value

)Note: The minimum value of brightness is 1 (darkest), and the maximum value is 100 (brightest)

7.2 Example：

Adjust the brightness to 100 (brightest)

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 06 64 00 2A 5A

Adjust the brightness to 50 (moderate)

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 06 32 00 7C 5A

Adjust brightness to 1 (darkest)

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 36 01 00 4F 5A

Mark：

1) After this brightness adjustment is completed (waiting for reply), the next brightness adjustment can be performed

8. Volume adjustment

8.1 Format

Frame-Head 31 sign Addr Data_L Data_H CRC 5A
Instruction :
Frame-Head: A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0
Sign: Execution sign, the single value register is 0xC0.
Addr: 0x5E
Data_L: Low byte of volume value
Data_H: High byte of volume value
CRC: XOR check value

Note: The minimum volume is 1 and the maximum is 100

In addition, you must ensure that the volume switch remains on when adjusting the volume

The volume switch is on：A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 5D 01 00 14 5A

The Volume switch off：A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 5D 00 00 15 5A

8.2 Example：

100 Volume adjust to 100

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 5E 64 00 72 5A

Volume adjust to 50

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 5E 32 00 24 5A

Volume adjust to 1

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 5E 01 00 17 5A

Mark：

2) The next volume adjustment can be done after the completion of this volume adjustment (waiting for reply)

9. Device output control

9.1 Format

Frame-Head 31 sign Addr Data_L Data_H CRC 5A

Instruction：

Frame-Head：A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0

Sign: Execution sign, the single value register is 0xC0.

Addr: 0x3C

Data_L: Low byte of output control

Data_H: High byte of output control

CRC: XOR check value

Description: output black screen 0, normal output 1

9.2 Example:

power on

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 3C 01 00 75 5A

Power off

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 3C 00 00 74 5A

Mark ：

3) The machine can be switched on and off the next time after the completion of this opening (waiting for reply)

10. Color temperature adjustment

10.1 Format

Frame-Head 31 sign Addr Data_L Data_H CRC 5A

Instruction ：

Frame-Head：A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0

Sign: Execution sign, the single value register is 0xC0.

Addr: 0x0B(Red) 0x0C(Green) 0x0D(Blue)

Data_L: Low byte of color temperature value
Data_H: High byte of color temperature value
CRC: XOR check value
Note: The minimum value of the color temperature is 1, the maximum value is 100

In addition, you must ensure that the color temperature mode is custom when adjusting the color temperature

Color temperature mode is custom mode：A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 0A 00 00 42 5A

10.2 Example：

Red:50

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 0B 32 00 71 5A

Green:50

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 0C 32 00 76 5A

Blue:50

A5 A5 A5 00 F1 10 F0 10 00 08 00 00 B0 31 C0 0D 32 00 77 5A

Mark：

4) The next color temperature adjustment can be done after this time (waiting for recovery)